IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: **Sailesh Chittipeddi, et al** Group Art Unit: **2825**

Application No.: **10/036,020** Examiner: **Keshavan, Belur V.**

Filed: **12/26/2001** Confirmation No.: **2451**

Atty. Docket No.: **Chittipeddi 89-14/075903-090**

Title: **CMOS Vertical Replacement Gate (VRG) Transistors**

TRANSMITTAL OF FORMAL DRAWINGS

June 3, 2004

Attention: Official Draftsperson
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir or Madam:

In response to the Examiner's Notice of Allowability and his request for corrected drawings, Applicant hereby submits formal drawings for the above-identified patent application. In the event there are any comments, to expedite this matter, please contact the undersigned directly at the telephone number listed below.

Respectfully submitted,

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CERTIFICATE OF MAILING

I HEREBY CERTIFY that this Transmittal of Formal Drawings is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 3rd day of June, 2004.

Pamela A. Pagel